Jingyuan (William) Li

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Education

University of California San Diego (UCSD) **Sep 2024 - Apr 2026**

M.S. in Electrical & Computer Engineering (Analog & Mixed-Singal Integrated Circuits Design)

GPA: 3.5/4.0

Courses: Analog IC Design, CMOS Circuits Design, IC Layout Design, Power Management IC Design, High-Speed Wireline Communications Circuits & Systems, Microwave Engineering, Communication Circuits Design, Biomedical IC Design

University of Glasgow (UoG) **Sep 2020 - Jun 2024**

B.Eng. in Electronic & Electrical Engineering (Dual-Degree)

GPA: First Class Honors

Courses: Microelectronics Systems, Circuits Analysis & Design, Embedded Processers, Artificial Intelligence & Machine Learning, Electronic Systems Design, Electronic Devices, Power Electronics, Control Engineering, VLSI Design, Team Deign Project & Skills

University of Electronic Science and Technology of China (UESTC) **Sep 2020 - Jun 2024**

B.Eng. in Electronic Information Engineering

GPA: 3.77/4.0 (Top 20%)

Courses: Physics, Fundamental Analog Circuits, Analysis & Design of Digital Logic, Signal & Systems, Digital Signal Processing, Electromagnetic Field & Microwave Technology, Final Year Project

Projects

Design of a 9-bit SAR ADC Layout in 65nm CMOS (Tape-Out) **Mar 2025 - Present**

Project Team Leader, UCSD

- Designed a clock-controlled comparator utilizing common-centroid layout and highly symmetrical metal routing, which achieved an input-referred offset below 1-bit resolution and a propagation delay under 600 ps under different process corners.
- Designed a unit MOM capacitor with capacitance of 5 fF through parasitic extraction, and built a 9-bit CDAC array based on common-centroid capacitor placement.
- Added dummy structures around the CDAC to ensure that the ratio between 2 adjacent bit capacitors was below 0.2%.
- Implemented the digital logic of the successive approximation algorithm in Verilog and generated the corresponding digital layout for the SAR logic control circuit using script-based automation.
- Designed a decoupling capacitor composed of NMOS transistors and 7 layers of crossed-finger metal.
- Completed the top-level chip schematic and Pad Ring layout, and verified full-chip DRC/LVS. Evaluated quantization and distortion noise of the SAR ADC under pre-fill, post-fill, and full-chip conditions, where the final SNR was tested to be 49 dB.
- Design a motherboard-daughter PCB system including COB package, power, SE-DE, buffers etc., for the SAR ADC testing.

Design of a 1.8V-to-0.8V DC-DC Buck Converter in 45nm CMOS **Feb 2025 - Present**

Project Manager, UCSD

- Created an ideal buck converter model to verify its feasibility and extracted unit switching transistor parameters using *Cadence*.
- Calculated ideal power conversion efficiency using *MATLAB*, and determined optimal transistor sizing and inductance based on a figure of merit which consisted of efficiency, power, and area of components.
- Designed a five-transistor error amplifier achieving a gain of 60 dB, and applied compensation to enhance the stability of the feedback network.
- Designed LDOs with 1V and 0.9V output, providing stable power supply for switches and digital circuits.
- Constructed a three-stage level shifter supporting voltage domains of 0-0.9V, 0.9-1.8V for PMOS and NMOS driving.
- Designed a ramp generator and PWM signal generator, which helped to produce control signals with appropriate frequency and duty cycle for a 0.8 V output.
- Simulate and optimize the closed-loop performance of the buck converter, achieving a power efficiency of 85.5% and a voltage ripple of 8.66 mV, with stable operation under different process corners currently.

Design of a 10 Gb/s Tunable Voltage-Mode Transmitter Driver with 3-Tap FFE in 65nm CMOS **Jua - Mar 2025**

Project Team Leader, UCSD

- Designed a transmitter driver with 3-tap FFE, reducing ISI in high-speed data transmission and improving signal integrity.
- Utilized *Cadence* to sample the pulse response of a channel under various data rates and developed a *MATLAB* program to calculate the FFE tap weights based on the sampled results and a zero-forcing algorithm.
- Designed a DAC circuit for each tap of the transmitter driver, where each tap had 5-bit resolution.
- Designed the transmitter to be in the single-ended and high-swing voltage driving mode using NRZ data format.
- Utilized foot transistors as switch to achieve tunable tap weights, enabling adaptability to different channel conditions.
- Constructed a receiver circuit based on continuous-time linear equalization, incorporating a strong-arm latch as the comparator in the decoding circuit.

Design of a Three-Stage Telescope Operational Amplifier Design in 65 nm CMOS **Sep - Dec 2024**

Project Manager, UCSD

- Designed an operational amplifier with a gain over 60 dB and a gain-bandwidth product close to 1 GHz for the transimpedance amplifier in a Bluetooth receiver, supporting a 0.5 V common-mode input and output.
- Adopted a Cascode - CS - CD structure with PMOS input; introduced Miller compensation between the first and second stages to meet high-gain and accurate bandwidth requirements.
- Calculated transistor dimensions, compensation capacitors, and nulling resistors based on process-library data such as carrier mobility, verified circuit feasibility, and iteratively optimized design parameters through DC and AC simulations.
- Constructed a common-mode feedback circuit forming a feedback loop between the output node and the NMOS current-source gate bias to stabilize the common-mode level and improve I/O linearity.
- Designed a constant-transconductance reference circuit to provide a stable bias current source, constructing the amplifier bias network using current mirrors and replica biasing.
- Achieved a gain of 61.6 dB, a gain-bandwidth product of 1 GHz, a phase margin of 73°, and a gain margin of 18 dB.

Internship

Teaching Assistant **Sep 2023 - Jul 2024**

James Watt School of Engineering, UoG

- Monitored 3 courses, including Microelectronics Systems, Circuits Analysis & Design, and Embedded Processors, responsible for question feedback, course tutorial delivery and assignment evaluation, etc., with a cover of over 1500 students.
- Customized comprehensive reviews on lecture materials and mock exam exercise for students as final exam preparation.
- Delivered lab instructions to students, including the utilization of SPICE software and basic applications of programming languages, etc.

Skills

- **Engineering:** Virtuoso (Advanced), Altium Designer (Skillful), LTSpice (Skillful), SolidWorks (Basic), MbedOS (Basic)
- **Programming:** MATLAB & Simulink (Advanced), Verilog (Skillful), Python (Basic), C (Basic)
- **Language:** Chinese (Native), English (IETLS 7), Japanese (Basic)
- **Efficiency:** Microsoft Office (Advanced)

Awards

First Class Scholarship for Excellent Students in UESTC (Top 10% in an Academic Year) 2021

Second Class Scholarship for Excellent Students in UESTC (Top 25% in an Academic Year) 2022, 2023